| Notice of Allowability | Application No. | Applicant(s) |
|---|---|---|
| | 10/774,599 | REESE ET AL. |
| | Examiner | Art Unit |
| | Nghia M. Doan | 2825 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *02/10/2004*.

2. ☒ The allowed claim(s) is/are *1 and 3-21 (renumbered 37 CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/08/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060120* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

VUTHE SIEK
PRIMARY EXAMINER

## DETAILED ACTION

1. Responsive to communication Applicant argument for application 10/774,599 filed on 02/10/2004, claims 1-21 are pending.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with attorney James M. Heintz, Reg. No. 41,828 on January 06th 2006.

The application have been amended as following:

Claim 1, line 3, after "a master arrival detection function" inserts "that is configured to output a feedback output".

Claim 1, line 6, after "a plurality of" inserts " input conductors for conducting a plurality of inputs".

Claim 1, line 8, after "wherein" deletes "said at least one block output is capable to being updated by".

Claim 1, line 9, after "compute function" inserts "is configured to update said at least one block output".

Claim 1, line 10, after "arrival detection function" changes "and" to "when".

Claim 1, line 10, after "compute function" changes "evaluating" to "evaluates".

Claim 1, line 11, after "true" changes ";" to ",".

Claim 1, line 12, before "said block" deletes "wherein said at least one block output is capable of being updated by".

Claim 1, line 13, after "compute function" inserts "is configured to update said at least one block output".

Claim 1, line 14, after "trigger arrival detection function," changes "and upon" to "when".

Claim 1, line 15, after "compute function" changes "evaluating" to "evaluates".

Claim 1, line 15, after "to false" inserts "; and wherein said master arrival detection function is configured to update said feedback output upon the arrival of all of said plurality of input".

Claim 2 is cancelled.

Claim 17, line 6, after "constructing a first circuitry set" changes "that implements" to "configured to implement".

Claim 17, line 8, after "phase select" inserts "signal".

Claim 17,line 9, after "constructing a second circuitry set" changes "capable of detecting" to "configured to detect".

Claim 17, line 10, after "trigger phase" inserts "original".

Claim 17, line 11, after "constructing a third circuitry set" changes "that implements" to "configured to implement".

Claim 17, line 14, after "constructing a fourth circuitry set" changes "capable of detecting" to "configured to detect".

Claim 17, line 15, after "trigger phase" inserts "signal".

Claim 17, line 15, deletes "wherein the output of said fourth circuitry set is".

Claim 17, line 15, before "a master phase" inserts "and outputs"

Claim 17, line 16, after "phase" inserts "signal which acts as a feedback output, when all of the master inputs and the trigger phase signal have arrived".

Claim 17, line 17, after "constructing a fifth circuitry set" changes "capable of selecting" to "configured to select".

Claim 17, line 17, after "trigger phase" inserts "signal".

Claim 17, line 18, after "phase select" inserts "signal".

Claim 17, line 18, before " said master phase" changes "capable of selecting" to "configured to select".

Claim 17, line 18, after " said master phase" inserts "signal".

Claim 17, line 19, after " a gate phase" inserts "signal".

Claim 17, line 20, after "constructing a sixth circuitry set" changes "capable of detecting" to "configured to detect".

Claim 17, line 20, after "the arrival of said gate phase" inserts "signal".

Claim 17, line 21, before "said gate phase" changes "latching" to "latch".

Claim 17, line 21, after "said gate phase" inserts "signal".

Claim 18, line 1, after " the method of claim 17," changes "further comprising the step of:" to "wherein said third set of circuitry is configured to".

Claim 18, line 2, before " said at least one new block" changes "updating" to "update".

Claim 18, line 2, after "one new block output" deletes "by said third set of circuitry".

Claim 18, line 4, after "phase select" inserts "signal".

Claim 19, line 1, after " the method of claim 17," changes "further comprising the step of:" to "wherein said third set of circuitry is configured to".

Claim 19, line 2, before " said at least one new block" changes "updating" to "update".

Claim 19, line 2, after "one new block output" deletes "by said third set of circuitry".

Claim 19, line 4, after "phase select" inserts "signal".

***Allowable Subject Matter***

3. Claims 1 and 3-21 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art of record does not teach or fairly suggest "a method for constructing an early evaluation, self-timed phased logic gate having a set of inputs and at least one current block output, said method comprising the steps of: selecting a subset of the set of inputs for which early evaluation can be performed as trigger inputs, wherein the remainder of the set of inputs are master inputs; constructing a first circuitry set configured to implement a first Boolean function based upon the value of said trigger inputs, wherein the output of said first circuitry set is a phase select signal; constructing a second circuitry set configured to detect the arrival of said trigger inputs, wherein the output of said second circuitry set

is a trigger phase original; constructing a third circuitry set configured to implement a second Boolean function based upon the value of at least said master inputs, wherein the output of said third circuitry set is at least one new block output; constructing a fourth circuitry set configured to detect the arrival of said master inputs and said trigger phase signal, and output a master phase signal which acts a feedback output, when all of the master input and the trigger phase signal have arrived; constructing a fifth circuitry set configured to select said trigger phase signal when said phase select signal is a first value, and configured to select said master phase signal when said phase select is a second value, wherein the output of said fifth circuitry set is a gate phase signal; and constructing a sixth circuitry set configured to detect the arrival of said gate phase signal and latch said gate phase signal and said at least one new block output, wherein the output of said sixth circuitry set is the at least one current block output".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Recited references the PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

VUTHE SIEK
PRIMARY EXAMINER